REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 1-104 were presented for examination.

Claims 2, 10, 12 and 77-82 were objected to due to use of the phrase "capable of". The claims have been amended to avoid use of this phrase. In view of the above changes, reconsideration and withdrawal of the objection to the above claims is respectfully requested.

The Office Action noted that claims 90 and 91 should depend from claim 74. Those claims have been amended to depend from claim 74.

Claims 69-71 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite. More specifically, these claims were rejected due to use of the phrase "wherein the means for generating", since the Office Action asserted it what not clear which means for generating was being referred to. The claims have been amended to obviate the grounds for this rejection. In view of the above changes, reconsideration and withdrawal of the rejection under § 112 are respectfully requested.

Claims 1-21, 23-64 and 66-104 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hartoog et al., "Generation of Software Tools from Processor descriptions for Hardware/Software Codesign". The grounds for this rejection are respectfully traversed.

Hartoog et al. describes a system in which software tools are developed based on a processor instruction set description in nML – see, e.g., Section 3, "Tools", where "[g]iven this kind of declarative description of an instruction set, it is possible to generate automatically several different useful tools. . .", namely, an instruction set simulator, a compiled instruction set simulator, a disassembler, an assembler, a code

generator, and a code retargeter." Hartoog generates software tools. It does not generate any hardware information, particularly a description of a hardware implementation of a processor as recited in claim 1. A method of use of the Hartoog et al. system would likely be to take an instruction description of a processor done by hand and use the Hartoog et al. system to produce a software tool chain for it more quickly than could be done by hand. There is nothing in Hartoog et al. about generating software tools and hardware from a common description.

Claims 13-21 recite various elements in the hardware description of claim 1. The Office Action asserts that all of these are inherent in the hardware description disclosed by Hartoog et al. Applicants again point out that Hartoog et al. fails to teach or suggest the generation of a hardware description, and disagree with the Office Action's statement. Should the Examiner maintain these rejections, Applicants respectfully request that the reason the features of each of elements 13-21 are deemed to be inherent in the description of Hartoog et al. be explained, so that Applicants may have a basis to discuss them. Similar comments apply to the asserted inherentness of claims 47-54.

Thus, claim 1 is not anticipated by the teachings of Hartoog et al. Claims 2-21, 23-64 and 66-103 depend from claim 1 and are allowable over Hartoog et al. for similar reasons. Claim 104 recites features similar to those of claim 1 and is allowable over Hartoog et al. for reasons similar thereto. In view of the above remarks, reconsideration and withdrawal of the rejection under § 102 are respectfully requested.

Claims 22 and 65 were rejected under 35 U.S.C. § 103(a) as being obvious in view of Hartoog et al. The grounds for this rejection are respectfully traversed.

Claims 22 and 65 depend from claim 1, and it has been shown that claim 1 is not anticipated by Hartoog et al. Inasmuch as Hartoog et al. also fails to suggest any of its shortcomings in relation to claim 1 as above, Applicants submit that claim 1 is not rendered obvious in view of Hartoog et al.

Since claim 1 is not rendered obvious in view of Hartoog et al., claims 22 and 65 depending therefrom similarly are not rendered obvious thereby. Thus, Hartoog et al. does not render these claims obvious. In view of the above remarks, reconsideration and withdrawal of the rejection under § 103 are respectfully requested.

Applicants note that the Office Action states that United States Patent No. 6,006,022 to Rhim et al. also teaches the present invention. Applicants suggest that if the Examiner believes this to be the case, the next Office Action should include one or more rejections based on Rhim et al. so that they will be able to address the reference properly.

All objections and rejections having been addressed it is respectfully submitted that the present application is now in a condition for allowance and a Notice to that effect is earnestly requested.

Respectfully submitted,
PILLSBURY MADISON & SUTRO LLP

By _____
Roger S. Joyner
Reg. No. 36,176

Tel. No.: (650) 233-4552
Fax No.: (650) 233-4040
Pillsbury Winthrop LLP
1600 Tysons Boulevard
McLean, Virginia 22102
Tel. (703) 905-2000

I certify that the enclosed papers and fee are being deposited with the U.S. Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on 11/07/01.

Margaret M. Hasson

APPENDIX

IN THE CLAIMS:

Please amend the claims as follows:

3. (Amended) The system of claim 1, wherein the [means for generating] software development tools [comprises means] are for generating software development tools [capable of generating] to generate code to run on the processor.

11. (Amended) The system of claim 9, wherein the instruction set simulator is [capable of modeling] to model execution of code being simulated to measure key performance criteria including cycles of execution.

12. (Amended) The system of claim 10, wherein the instruction set simulator is [capable of profiling] to profile execution of the program being simulated to record standard profiling statistics, including a number of cycles executed in each simulated function.

69. (Amended) The system of claim 1 wherein the means for generating a description of a hardware implementation of the processor is further for providing a characterization of hardware performance and cost, and the means for generating the software development tools are for generating software application performance information together with the means for generating a description of a hardware implementation of the processor, to facilitate modification of the configuration specification.

70. (Amended) The system of claim 1 wherein the means for generating a description of a hardware implementation of the processor is further for providing a characterization of hardware performance and cost, and the means for generating the software development tools are for generating software application performance information together with the means for generating a description of a hardware implementation of the processor, to facilitate an extension of the configuration specification.

71. (Amended) The system of claim 1 wherein:

the means for generating a hardware description of the processor is further for providing a characterization of hardware performance and cost, and the means for generating the software development tools are for generating software application performance information together with the means for generating a description of a hardware implementation of the processor, to facilitate modification of the configuration specification[,]; and

the means for generating a hardware description of the processor is for providing a characterization of hardware performance and cost, and the means for generating the software development tools are for generating software application performance information together with the means for generating a description of a hardware implementation of the processor, to facilitate the description of an extension of the configuration specification.

77. (Amended) The system of claim 75, wherein the software development tools include a compiler [capable of generating] to generate the user-defined instruction.

78. (Amended) The system of claim 77, wherein the compiler is [capable of optimizing] to optimize code containing user-defined instructions.

79. (Amended) The system of claim 75, wherein the software development tools include an assembler [capable of generating] to generate the user-defined instruction.

80. (Amended) The system of claim 75, wherein the software development tools include a simulator [capable of simulating] to simulate execution of user code using the user-defined instruction.

81. (Amended) The system of claim 75, wherein the software development tools include tools [capable of verifying] to verify the user implementation of the user-defined instruction.

82. (Amended) The system of claim 74, wherein the compiler is [capable of] to automatically [generating] generate additional instructions.

90. (Amended) The system of claim [73] 74, wherein the additional structure adds no new state to the processor.

91. (Amended) The system of claim [73] 74, wherein the additional instruction adds state to the processor.